REMARKS

The present Amendment is in response to the Examiner's Final Office Action mailed July 10, 2008. Claim 9 is amended. Claims 1- 26 remain pending.

Reconsideration of the application is respectfully requested in view of the above amendments to the claims and the following remarks. For the Examiner's convenience and reference, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. General Considerations

Applicants respectfully note that the remarks herein do not constitute, nor are they intended to be, an exhaustive enumeration of the patentable distinctions between any cited references and the invention, example embodiments of which are set forth in the claims of this application. Rather, and in consideration of the fact that various factors make it impractical to enumerate all the patentable distinctions between the invention and the cited art, as well as the fact that the Applicants have broad discretion in terms of the identification and consideration of the base(s) upon which the claims distinguish over the cited references, the distinctions identified and discussed herein are presented solely by way of example. Consistent with the foregoing, the discussion herein is not intended, and should not be construed, to prejudice or foreclose contemporaneous or future consideration by the Applicants, in this case or any other, of: additional or alternative distinctions between the invention and the cited references; and/or, the merits of additional or alternative arguments.

Applicants note as well that the remarks, or a lack of remarks, set forth herein are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicants reserve the right to challenge the purported teachings and purported prior art status of the cited references at any appropriate time.

II. Claim Rejections Under 35 U.S.C. § 102

Applicant respectfully notes that a claim is anticipated under 35 U.S.C. § 102(a), (b), or (e) only if each and every element as set forth in the claim is found, either expressly or inherently

described, in a single prior art reference. Further, the identical invention must be shown in as complete detail as is contained in the claim. Finally, the elements must be arranged as required by the claim. *Manual of Patent Examining Procedure ("MPEP") § 2131.*

The Examiner has rejected claim 14 under 35 U.S.C. § 102(e) as being anticipated by United States Patent Publication No. 2004/0179138 to *Wang et al.* ("*Wang*"). Applicants respectfully traverse the rejection.

Claim 14 recites, among other things:

> receiving an asserted synchronization signal from a phase locked loop…
>
> determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency; and
>
> asserting a lock signal if the phase locked loop has locked onto a data signal.

Applicants note at the outset that the Examiner has again failed to specifically identify which portion(s) of *Wang* are believed by the Examiner to correspond to the claimed "**determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency**," and has essentially repeated the rejection set forth in the Office Action mailed October 5, 2007. While this shortcoming in the rejection was clearly identified in Applicant's paper filed February 28, 2008, the Examiner has nonetheless failed to respond, in the Office Action mailed July 10, 2008, to the points advanced by Applicants in that paper.

The failure of the Examiner to address Applicant's prior arguments is contrary to established examination guidelines. Particularly, Applicant notes that "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, *take note of the applicant 's argument and answer the substance of it*." *M.P.E.P. § 707.07(f)* (emphasis added).

With regard to the continued failure of the Examiner to particularly identify what the Examiner believes to be the correspondence between *Wang* and the aforementioned elements of claim 14, Applicants submit that if the origin of teachings that allegedly anticipate claim 14 are believed by the Examiner to be present in *Wang*, then Applicants request that this origin be set forth as suggested by MPEP 2144.08 III which states, "[w]here applicable, the finding should clearly articulate which portions of the reference support any rejection. Explicit findings on

motivation or suggestion to select the claimed invention should also be articulated in order to support a 35 U.S.C. 103 ground of rejection. *Dillon*, 919 F.2d at 693, 16 USPQ2d at 1901; *In re Mills*, 916 F.2d 680, 683, 16 USPQ2d 1430, 1433 (Fed. Cir. 1990). Conclusory statements of similarity or motivation, without any articulated rationale or evidentiary support, do not constitute sufficient factual findings." (Emphasis added.)

Moreover, in the response to arguments section of the Office Action, the Examiner made inconsistent assertions as to what element(s) in *Wang* correspond to the claimed "synchronization signal." In particular, the Examiner identified the claimed "synchronization signal" as corresponding to each of the following: 1) "the output from the PLL [3] to the detection signal" and 2) "the output of the PLL [3] (input to the separator 5)."[1] *See Office Action*, p. 3. Therefore, Applicants respectfully request clarification as to **which of the aforementioned PLL output signals is believed by the Examiner to correspond to the claimed "synchronization signal."**

Assuming the Examiner's position is that a signal passed to PLL detection circuit 17 is the claimed "synchronization signal," the Examiner has not established that *Wang* teaches determining whether such a signal "is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed. For example, the Examiner alleged, "Based on the output from the PLL circuit, label 3, the detection circuit label 17 outputs a PLL_S to indicate the locked status of the PLL, label 3." *See Office Action*, p. 3. However, this statement does not even assert, much less establish, that *Wang* teaches determining whether the output from the PLL circuit 3 is "caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed.

Similarly, if the Examiner's position is that a signal passed to separator 5 is the claimed "synchronization signal," the Examiner has not established that *Wang* teaches determining whether such a signal "is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed. For example, the Examiner alleged "it is well known…that determining whether the PLL is locked or

[1] In referring to "the output from the PLL [3] to the detection signal," the Examiner appears to be referring to an output that is inherently sent from PLL 3 to "PLL detection circuit 17." (Emphases added.) If such understanding is incorrect, clarification is respectfully requested.

unlocked must be determined by using output of the PLL." *See Office Action*, p. 3. However, this statement does not even assert, much less establish, that *Wang* teaches determining whether the output sent from PLL 3 to separator 5 "is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency."

Therefore, Applicants respectfully request additional clarification as to: 1) **what signal in *Wang* purportedly corresponds to the claimed "synchronization signal"** and 2) **where *Wang* allegedly discloses "determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency**," as claimed.

Since the Examiner has failed to establish that *Wang* discloses each and every element of claim 14, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

III. Claim Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 1-3, 9, 10, and 15 under 35 U.S.C. § 103 as being unpatentable over *Wang* in view of "The 555 Timer Tutorial" by Tony van Roon ("*van Roon*"); rejected claims 4 and 5 under 35 U.S.C. § 103 as being unpatentable over *Wang* in view of *van Roon* as applied to claim 3 above and further in view of "Transistors" at www.electronics-tutorials.com ("*Transistors Tutorial*"); rejected claims 16 and 17 as being unpatentable over *Wang* as applied to claim 14, and further in view of U.S. Patent No. 5,886,748 to *Lee* ("*Lee*"); rejected claims 6, 7, 11, and 12 as being unpatentable over *Wang* and *van Roon* as applied to claim 2, and further in view of *Lee*; rejected claim 8 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 7, and further in view of "Phase-Locked Loop Protocol Scheme for a Synchronization Field," IBM Technical Disclosure Bulletin, May 1990 ("*IBM TDB*"); rejected claim 13 as being unpatentable over *Wang*, *van Roon*, and *Lee*, as applied to claim 12, and further in view of *IBM TDB*; and rejected claim 18 as being unpatentable over *Wang* as applied to claim 14, and further in view of *IBM TDB*.

The Examiner has also rejected claims 19 and 20 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,794,944 to *Hirai* ("*Hirai*") in view of *van Roon*; rejected claim 21 as being unpatentable over *Hirai* and *van Roon*, as applied to claim 20, and further in

view of *Transistors Tutorial*; and rejected claims 22-26 as being unpatentable over *Hirai* and *van Roon*, as applied to claim 19, and further in view of *IBM TDB*.

For at least the reasons set forth below, Applicant respectfully traverses each rejection.

A. Claims 1-8

Claim 1 recites, among other things, "...a phase locked loop adapted to...keep [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and a timing circuit adapted to measure a period of time that the synchronization signal is asserted and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time."

The Examiner asserted that *Wang* discloses a circuit that produces a lock signal if a synchronization signal is asserted for at least a pause time, Tp. *See Office Action*, p. 8. However, as with claim 14 discussed above, it is unclear from the Examiner's response **what portion of *Wang* is believed by the Examiner to correspond to the claimed "synchronization signal**." Thus, **clarification on this point is respectfully requested**.

Furthermore, Applicants previously raised the following argument, which was not acknowledged or answered in the Office Action:

> Moreover, as the name "pause time" implies (*see Wang*, paragraph [0051]), time Tp is merely used to pause an activity, to allow "coincidence detection circuit 7 to detect whether synchronization of the horizontal oscillator 8 with the incoming RF signal has been achieved...." *See Wang*, paragraph [0043]. As presently understood then, the pause time, Tp, is not used as a "specified period of time" to be measured against "a period of time that the synchronization signal is asserted," as required by claim 1.

See Applicants' paper filed February 28, 2008, p. 13.

The failure of the Examiner to address the aforementioned argument is contrary to established examination guidelines. Particularly, Applicant notes that "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, *take note of the applicant 's argument and answer the substance of it*." *M.P.E.P. § 707.07(f)* (emphasis added).

In light of the foregoing remarks, the Examiner has failed to establish that *Wang* teaches or suggests each and every element of claim 1. Furthermore, the Examiner has not established that any of *van Roon*, *Transistors Tutorial*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim elements, would cure the deficiencies of *Wang*. Accordingly,

Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness and respectfully submit that the rejection of claim 1, and corresponding dependent claims 2-8, should be withdrawn.

B. Claims 9-13

Amended claim 9 recites, among other things:

> a controller chip having a phase locked loop that ... is adapted to operate in a locked mode in which the phase locked loop asserts the synchronization signal so long as the phase locked loop is locked onto a data signal; and
>
> a translation circuit adapted to convert the synchronization signal from the controller chip to a lock signal usable by the host device, wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal and is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode.

In contrast, the Examiner has not established that *Wang* discloses the aforementioned elements. The Examiner asserted, "As per the rebuttal above [with respect to claim 14], the examiner points the applicant in the direction of paragraphs 33 and 35, wherein such paragraph describes the translation circuit." *See Office Action*, p. 5. However, "the rebuttal" referred to by the Examiner does not clearly identify what is believed by the Examiner to correspond to the claimed "translation circuit," nor do "paragraphs 33 and 35" of *Wang*.

For example, although the Examiner's analysis is vague on this point, it may be that the Examiner believes detection circuit 17 corresponds to the claimed "translation circuit." However, the Examiner has not even asserted, much less established, that detection circuit 17 is "adapted to convert the synchronization signal from the controller chip to a lock signal usable by the host device," as claimed, or that "a logic level of [a] lock signal [from detection circuit 17]...is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode," as claimed. (Emphases added.)

Moreover, the Examiner has not shown that the deficiencies of *Wang* are cured by *Van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim elements. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case for obviousness with respect to claim 9 and therefore submit that the rejection of claim 9, and corresponding dependent claims 10-13, should be withdrawn.

C. Claims 15-18

Applicants respectfully submit that insofar as the rejections of claims 15-18 rely on the unsupported assertions regarding the disclosure of *Wang* advanced by the Examiner in connection with the rejection of claim 14, such rejection lacks an adequate foundation, for at least the reasons outlined at section II above. Furthermore, the Examiner has not shown that *van Roon*, *Lee*, and *IBM TDB*, each relied on for their alleged teaching of various other claim elements, would cure the deficiencies of *Wang*. Accordingly, the rejections of claims 15-18 should be withdrawn.

D. Claims 19 and 20

Claim 19 requires, among other things, "a timing circuit...and a comparator circuit adapted to compare the output signal [from the timing circuit] with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time."

In rejecting claim 19, the Examiner identified a comparison circuit 23 in *Hirai* as the claimed "comparator circuit." *See Office Action*, p. 15. The Examiner conceded that *Hirai* does not disclose the claimed "timing circuit." *See id.*, p. 16. However, according to the Examiner, *van Roon* discloses a timing circuit (a 555 timer) and "it would have been obvious to use the timer...in the invention of Hirai." *See id.*, pp. 16 and 17. Applicants respectfully disagree. As argued by Applicants previously:

> As presently understood then, the combination proposed by the Examiner would result in a configuration where the comparison circuit 23 of *Hirai* would compare a count value from one of counters 21 and 22 with the timing pulse from the *van Roon* timing circuit. However, it is not apparent that a count value (*Hirai*) is the same as a timing pulse (*van Roon*), nor has the Examiner established as much. Thus, the comparison performed by the modified circuit 23 of *Hirai* would not be feasible and/or would at best yield meaningless results and the device would be unsatisfactory for its intended purpose of optimizing a lock detection time. *See Hirai*, Abstract.

See Applicants' paper filed February 28, 2008, pp. 15 and 16 (emphasis in original).

In the response to arguments section of the Office Action, the Examiner acknowledged the foregoing arguments but did not answer the substance of them. Specifically, **the Examiner**

did not address the incompatibility of combining the timer of *van Roon* with the comparison circuit 23 of *Hirai*. Instead, the Examiner asserted that the comparison circuit 23 of *Hirai* could be viewed as "comparing the transitions from...two signals," as opposed to comparing count values, and that claim 19 "does not indicate the reference signal and the feedback cannot be altered or changed in form." *See Office Action*, p. 6 (emphasis added).

Moreover, according to the Examiner, the feedback signal in *Hirai* is a "timing signal." *See Office Action*, p. 6 ("Fig. 1 shows the counters provide a count value based on...feedback or timing signal (label feedback signal.") However, in asserting that the feedback signal is a "timing signal" the Examiner now appears to have taken a position opposite the one taken in the rejection, namely, that "*Hirai* fails to disclose...a timing circuit that measures a period of time that a signal is asserted." *See Office Action*, p. 16 (emphasis added). Therefore, **clarification is respectfully requested as to the Examiner's position on this point**. In addition, should the Examiner determine that the feedback signal of *Hirai* is a "timing signal" produced by a timing circuit, Applicants respectfully request that the Examiner **specifically identify what element in *Hirai* is believed to correspond to the claimed "timing circuit that measures a period of time that [a signal] is asserted**."

Therefore, the rejections based on the purportedly obvious combination of *Hirai* and *van Roon* are deficient in at least the foregoing respects. Furthermore, the Examiner has not shown that the deficiencies would be cured by *Transistors Tutorial* or *IBM TDB*, each relied on for its alleged teachings of various other claim elements. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness and respectfully request that the rejection of claim 19, and corresponding dependent claims 20-26, be withdrawn.

IV. Fee Payment

The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; and/or (2) any patent application and reexamination processing fees under 37 CFR § 1.17; and/or (3) any post issuance fees under 37 CFR § 1.20. In addition, if any additional extension of time is required, which has not otherwise been requested, please consider this a petition therefor and charge any additional fees that may be required to Deposit Account No. 23-3178.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that each of the pending claims 1-26 is in condition for allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 10th day of October, 2008.

Respectfully submitted,

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